Surface-Mounted GaAs Active Splitter and Attenuator MMIC's Used in a 1–10-GHz Leveling Loop

GARY S. BARTA, KEITH E. JONES, GEOFFREY C. HERRICK, AND ERIC W. STRID, MEMBER, IEEE

Abstract—**A wide-band monolithic GaAs bridge-T variable attenuator has been used with a monolithic GaAs active power splitter to form a compact 1–10-GHz leveling loop having a minimum 9-dB leveling range with buffered output. The attenuator internally optimizes input and output return loss over a 1–10-GHz bandwidth by the use of an on-chip GaAs op-amp. The active power splitter provides unity gain to each port over a 1–10-GHz bandwidth by the use of distributed amplification. The entire 4.5-cm by 4.2-cm subsystem was realized with surface mount packages on RT-Duroid®, demonstrating new construction techniques for GaAs MMIC assembly.**

I. Introduction

GALLIUM-ARSENIDE MMIC's have recently ventured from the development stage into the marketplace. The majority of MMIC's currently available are gain blocks, with only a few exceptions. The additional microwave "building blocks" are not yet available, mainly because of the application-specific nature of microwave design. Because GaAs MMIC's need to address a broad spectrum of applications and bandwidths, standard function MMIC's must be carefully chosen. Otherwise, the volume of MMIC's will not realize the lower price per component which is one of the major goals of moving circuits to the monolithic level. Two such generic microwave components are exemplified here in a practical, broadband microwave leveling loop.

The design approach used allowed a broad bandwidth operation of 1 to 10 GHz for both the attenuator and splitter MMIC's. The MMIC's were fabricated with a high-yield, 1-μm GaAs depletion mode ion-implantation process [1], incorporating NiCr resistors for stable terminations and MIM capacitors for on-chip bypassing and decoupling. The inductors used second-layer air-bridge metal to reduce skin effect losses and increase the self resonant frequency. Both parts were designed for operation from a single 9–15-V power supply for ease of use and incorporation into existing system environments. A die size of 54 by 43 mil was chosen for both circuits to fit into a hermetic, surface mount microwave package.

A major obstacle to the realization of GaAs MMIC utility is high-speed packaging. MMIC's can offer low cost, small size, and high-frequency performance, but fundamental changes to the current methods of intricate milled enclosures and glass-to-metal seals for microwave subsystems are required. The microwave package shown here follows the current trend of small, low-cost, surface mount packaging techniques and offers a solution to the MMIC packaging dilemma.

The design and performance of each of the MMIC's are described separately, and together in the leveling-loop application, demonstrating the packaging and use of broad-band MMIC's in microwave subsystems.

II. Variable Attenuator

Gain control of amplifier cascades generally requires a variable attenuator element. For amplifier gain flatness and stability, it is desirable that the attenuator provide low source and load VSWR regardless of the attenuation value. This precludes reflective attenuator topologies. The classic bridged-T attenuator [2], shown in Fig. 1, becomes a continuously variable absorptive attenuator when R_1, the series bridging resistance, and R_2, the shunt resistance, are allowed to vary as follows:

$$R_1 R_2 = Z_0^2 \tag{1}$$

where Z_0 is the desired characteristic impedance. The attenuation when matched is given by

$$\begin{aligned}\text{attenuation (dB)} &= 20\log\left((R_1/R_2)^{1/2}+1\right)\\ &= 20\log\left((R_1/Z_0)+1\right).\end{aligned} \tag{2}$$

By replacing the series and shunt resistances R_1 and R_2 with FET's operating in the linear region, as in Fig. 1, a monolithic implementation of the bridged-T attenuator, shown in Fig. 2, has been realized. The channel resistance of a FET in the linear region can be varied by V_{gs}, and is essentially $1/g_{m_{SAT}}$, where $g_{m_{SAT}}$ is the transconductance from the saturated region

$$I_{ds} \approx 2\frac{W}{L}\beta_0\left(V_{gs}-V_p\right)V_{ds} \approx g_{m_{SAT}}V_{ds} \tag{3}$$

Manuscript received May 13, 1986; revised August 25, 1986.

G. Barta is with TriQuint Semiconductor, Inc., Tektronix Industrial Park, P.O. Box 4935, Group 700, Beaverton, OR 97076.

K. Jones and G. Herrick are with Tektronix, Inc., P.O. Box 500, MS 58-204, Beaverton, OR 97077.

E. Strid is with Cascade Microtech, Inc., P.O. Box 2015, Beaverton, OR 97075.

IEEE Log Number 8611163.

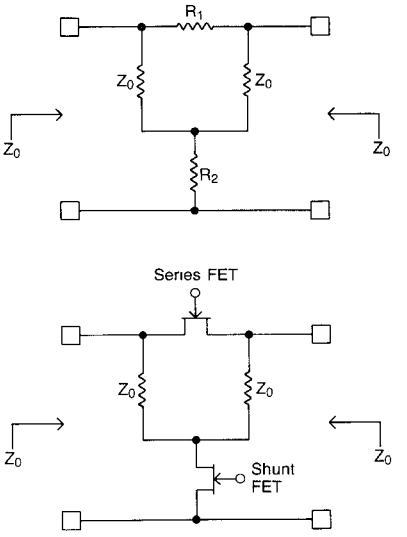


Fig. 1. The bridged-T attenuator (upper) shown with the series and shunt elements replaced with MESFET's (lower).

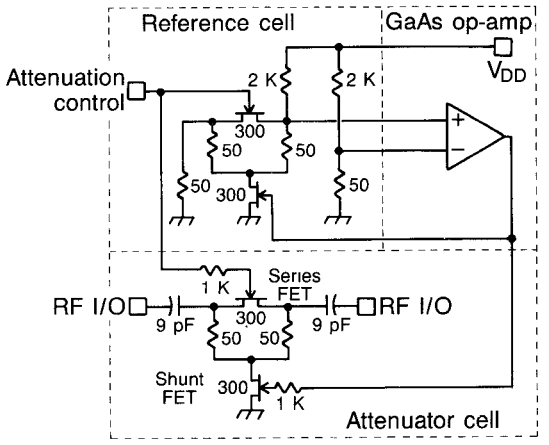


Fig. 2. Monolithic 1–10-GHz variable attenuator using GaAs FET's in the bridged-T configuration with on-chip return-loss optimizing circuitry. Input protection and level shifting circuits on the control input are not shown.

where W and L are the FET gate width and length, respectively, and V_p is the pinchoff voltage. The transconductance parameter β_0 is given as $\beta_0 \approx (\mu\epsilon_s/2a)$, where μ is the channel electron mobility, ϵ_s is the permittivity of the GaAs, and a is the channel thickness [3]. It can be seen from (3) that the channel resistance $(\partial I_{ds}/\partial V_{ds})^{-1}$ is dependent on GaAs process spreads, through both β_0 and V_p. The task then is to control the product of series and shunt channel resistances for proper attenuator operation. Solving for the necessary applied FET voltages yields the following relation (between series and shunt gate voltages V_{gs_1} and V_{gs_2}), for maintaining good return loss at any given attenuation for FET's of equal geometry

$$(V_{gs_2} - V_p) = \frac{L^2}{4W^2\beta_0^2 Z_0^2 (V_{gs_1} - V_p)}. \quad (4)$$

At low frequencies, the attenuation for equal geometry

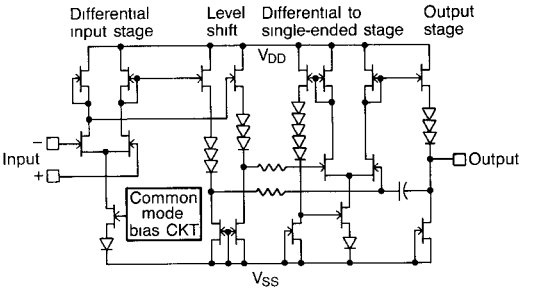


Fig. 3. Schematic diagram of the GaAs operational amplifier used in the MMIC attenuator.

series and shunt FET's when (4) is satisfied is

$$\text{attenuation (dB)} = 20\log\left\{\left(\frac{V_{gs_2} - V_p}{V_{gs_1} - V_p}\right)^{1/2} + 1\right\}$$

$$= 20\log\left(\frac{L}{2W\beta_0 Z_0 (V_{gs_1} - V_p)} + 1\right). \quad (5)$$

Fortunately, feedback can be used to control input and output return loss as attenuation is changed, invariant of any process effects or differences between FET geometries. Fig. 2 shows the reference attenuator cell where an operational amplifier maintains a 50-Ω environment by adjusting the shunt FET gate voltage in response to an arbitrary voltage variation on the series FET gate. Before the MMIC attenuator was designed, the concept of using reference cell dc parameter feedback to control the RF cell was verified by using two GaAs FET bridged-T attenuators and a 741 operational amplifier. This concept was carried to the monolithic level by implementing the op-amp on chip. Using dc parameters requires that enough voltage be applied to the reference attenuator cell to obtain a usable signal level for the op-amp to measure, but not enough that the FET's leave the linear region. In this design, FET drain–source voltages were kept below 200 mV.

Fig. 3 shows a schematic diagram of the GaAs operational amplifier used in the attenuator design. It consists of two gain stages, an input differential pair and a differential-to-single-ended (DSE) stage, providing approximately 50 dB of open-loop gain. The DSE stage is commonly used in NMOS designs, and was recently verified in GaAs depletion mode technology [4]. Since high-frequency performance was not the goal of this amplifier, stability was ensured by excess dominant pole compensation, limiting the bandwidth to under 100 MHz.

Several factors have to be considered when using FET's for the shunt and series elements. FET widths must be chosen wide enough for low insertion loss in the minimum attenuation state, but small enough to limit parallel drain-to-source capacitance C_{ds} so that the isolation at higher frequencies is sufficient in the maximum attenuation state. Both series and shunt widths were chosen as 300 μm. The maximum attenuation is most dependent on the C_{ds} of the series FET, so this device was built as a single gate finger device to reduce additional drain-to-source capacitance

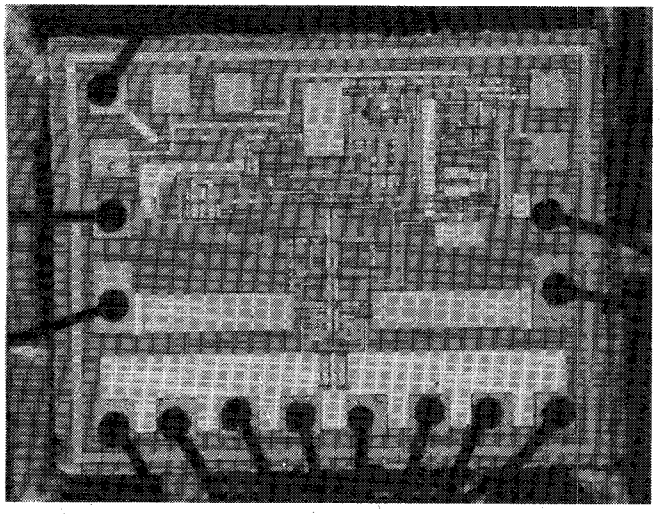


Fig. 4. Microphotograph of the 1–10-GHz variable attenuator. The op-amp is visible in the upper right corner.

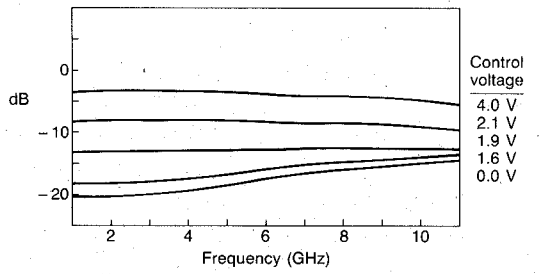


Fig. 5. Attenuation versus frequency for varying control voltages.

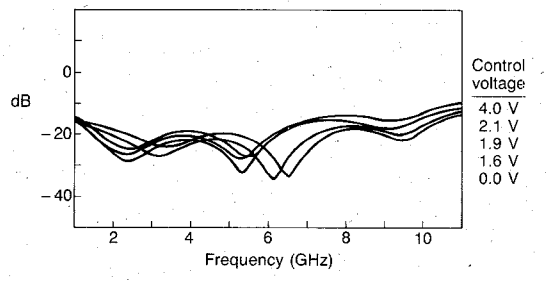


Fig. 6. Input return loss versus frequency for various attenuations using on-chip return-loss optimization scheme.

caused by the interconnection parasitics which occur in interdigitated structures. The losses associated with the metal resistance of the single gate finger series device do not affect the RF performance of the attenuator. A photograph of the attenuator MMIC is shown in Fig. 4.

Fig. 5 shows the transmission characteristics of the packaged attenuator. The gain slope at minimum attenuation is caused by combined skin effect losses due to the package and to the microstrip structures on the GaAs from the edges of the die to the RF attenuator cell. Minimum attenuation is 3.5 dB at 1 GHz, increasing to 5 dB at 10 GHz. In this design, the gate-to-source voltage V_{gs} of both FET's was never allowed to be positive. If V_{gs} is allowed to go positive near the forward conduction point, the minimum attenuation will improve by approximately 1 dB. The effect of C_{ds} of the series FET upon the maximum attenuation increases visibly at higher frequencies. The

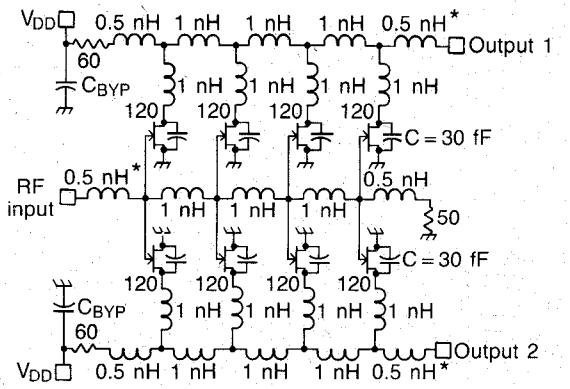


Fig. 7. Active splitter using distributed topology and common input gate line. Elements marked with * include bond wires.

attenuation range is 17 dB at 1 GHz, decreasing to 10 dB at 10 GHz.

Fig. 6 shows the return loss of the packaged part as a function of frequency using the on-chip correction circuitry. Return loss exceeds 12 dB over the 1–10-GHz band, translating to a better than 1.7:1 VSWR. This performance demonstrates that the addition of complex analog biasing circuits can be used to bring increased functionality to GaAs MMIC designs.

III. Active Power Splitter

The active power splitter provides unity gain to each port over the 1–10-GHz band through the use of distributed amplification. Other reported active splitter approaches have resulted in narrow-band operation [5], [6]. As shown in Fig. 7, two distributed amplifiers share a common input line to provide dual outputs without the need for lossy resistive or band-limiting reactive dividers. This technique can also be used as an active power combiner by using a shared output drain line [7]. The inherent symmetry of the topology provides close amplitude and phase match between outputs. This concept, in theory, can be extended to N outputs or, with dual-gate FET's, to switchable outputs. Unequal power division is possible with unequal side to side FET periphery. In this way, active couplers can be realized with wider bandwidths and lower losses than are possible with passive implementations.

The combined input capacitance of two 120-μm-wide FET's forms the shunt reactance element for each section of the lumped equivalent 50-Ω input line. The four sections have a total gate periphery of 480 μm per side. The devices operate at I_{DSS} for maximum power gain and require 100 mA total current from a single 8–15-V power supply. FET gate–drain spacings were increased to 2 μm for increased voltage breakdown, and FET's were spread out over the die area with only two fingers interdigitated at their closest spacings to minimize channel temperatures. A maximum gain from the input to either output of 1.3 dB is possible before including finite inductor Q and packaging losses. These losses were partially compensated at the high end by adding a series inductance on each drain to peak the overall response and introduce some slight positive gain

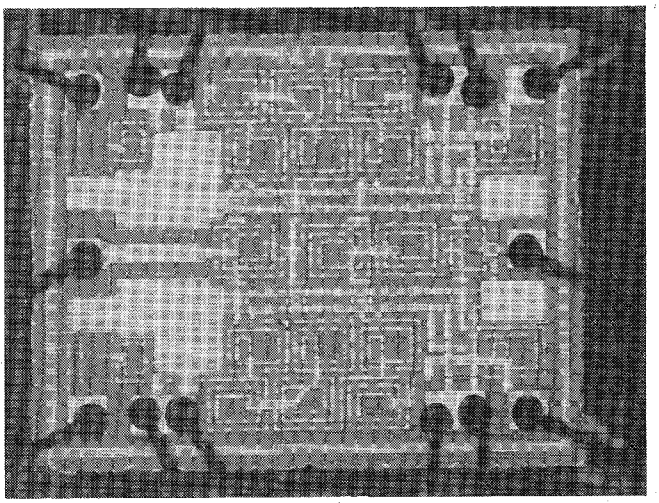


Fig. 8. Microphotograph of the 1–10-GHz active power splitter.

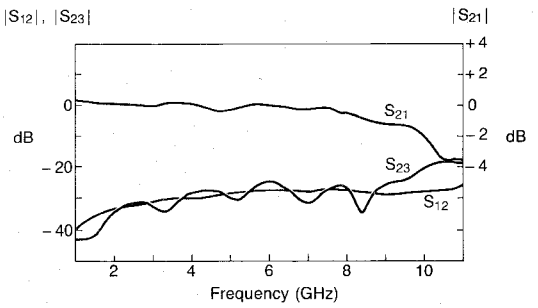


Fig. 9. Active splitter transmission characteristics. Note that S_{21} is shown at 2 dB/div. Output port-to-port isolation S_{23} and reverse isolation S_{12} are at 10 dB/div.

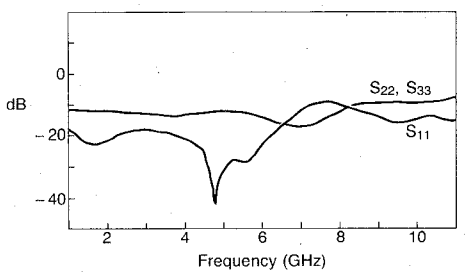


Fig. 10. Active splitter reflection characteristics.

slope in the unpackaged part. This peaking occurs from the inductors tending to impedance match the FET outputs at high frequencies. Since the FET drain conductances periodically load the output line, increasing the reverse drain termination resistor to 60 Ω improved the output match. Fig. 8 shows a photo of the splitter MMIC.

Fig. 9 shows the transmission characteristics of the packaged splitter. Gain flatness was ±1 dB over 1 to 10 GHz, and less than ±0.5 dB over the 2–8-GHz band. Output port-to-port isolation S_{23} exceeded 24 dB up to 9 GHz, decreasing to 20 dB at 10 GHz. One-dB compressed power output was measured to be greater than +10 dBm at 8 GHz at $V_{DD}=10$ V. Reverse isolation was greater than 27 dB from 1 to 10 GHz. Packaged input and output VSWR's, shown in Fig. 10, were better than 2:1, typical of the broad-band performance of distributed amplifiers.

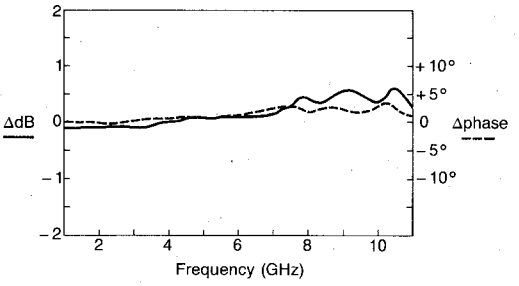


Fig. 11. Packaged active splitter phase and amplitude balance between output ports.

Packaged output amplitude and phase balances over 1 to 10 GHz were less than ±0.4 dB and ±1.5°, respectively, and are illustrated in Fig. 11. The excellent phase and amplitude match is due to the symmetry incorporated into the active splitter topology, as well as to the surface mount package design.

IV. Surface Mount Package

A low-cost, hermetic package was designed to accept the attenuator and active splitter, as well as other GaAs MMIC's [8]. A surface mount configuration was chosen to allow interconnection of the devices on Teflon etched circuit boards instead of the thin-film chip and wire technology used with discrete FET's and MMIC's. This approach permits simplified parametric testing of each completed MMIC device prior to assembly, simplified module assembly and rework, and the ability to reduce coaxial cable interconnects.

The package consists of a 0.310-in by 0.310-in thin-film ceramic hybrid circuit brazed to both an etched Kovar leadframe and a tungsten/copper thermal button, as shown in Fig. 12. A drawn metal cover completes the assembly after die attach and wirebond. The package accommodates one MMIC and up to two bypass capacitors in a hermetically sealed environment. Eight high-frequency lines and 12 grounds are arranged in a ground–signal–ground format for connection to the circuit board. Overall package dimensions are 0.410-in square. The package is joined to the Teflon ECB with solder lap joints, with the thermal button providing a conduction path through the ECB to an aluminum backing plate. Measured thermal resistance is less than 35°C/W from die attach pad to an aluminum backing plate in still air. The package was designed to handle 1–1.5-W dissipation levels when provided with an appropriate heat sink.

A surface mount package requires that the signal path transition from the package backside to the topside bonding surface. Modeling of a plated substrate via revealed the possibility of a transition from compensated microstrip to coplanar waveguide (CPW). The capacitance of the via hole cylinder to the ground plane can be compensated by short inductive sections entering the hole from both the ground plane CPW side and topside microstrip (Fig. 13). This forms a T section low-pass network. The inductive sections can be simultaneously adjusted without changing the width of the signal lines by simply varying the width of

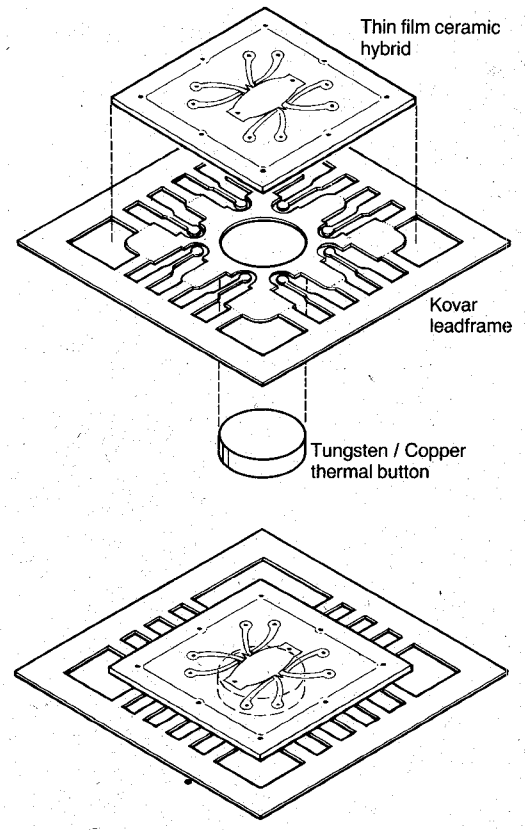


Fig. 12. Microwave surface-mount package explosion.

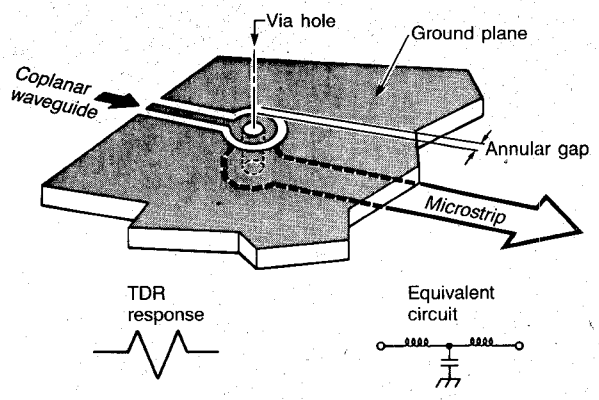


Fig. 13. Surface mount package signal transition. For clarity, the substrate is shown inverted. (Die attaches to microstrip side.)

the ground plane via hole annulus. Preliminary geometries of the transmission lines and "compensated via" were developed using SuperCompact®. The final geometries were developed using 100× scale models and verified by time-domain reflectometry. The package transition provides a 20-dB return loss between the Teflon ECB and the die at frequencies up to 12 GHz. Through-insertion loss is less than 1 dB at 12 GHz, as shown in Fig. 14. These results were obtained by using a test board which permits error-corrected vector measurements, allowing the measurement reference plane to be moved to the package leadframe. Thus, the response of the package test fixture is removed.

Fabrication of the package consists of brazing the leadframe and thermal button to the thin-film hybrid and Ni–Au plating the assembly. Metallized via holes are

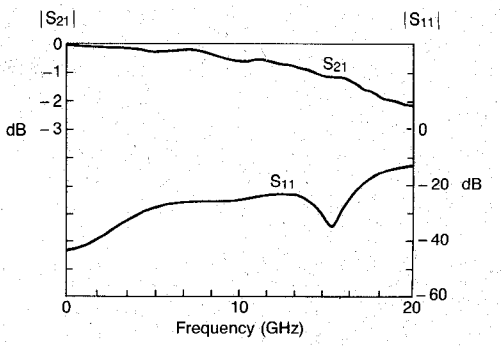


Fig. 14. Measured package transmission and reflection characteristics.

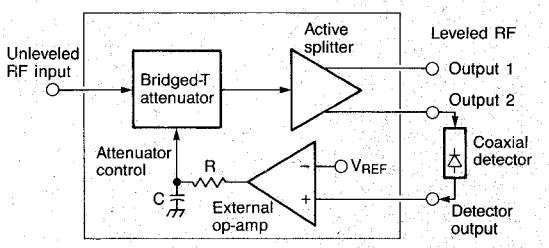


Fig. 15. Block diagram of the leveling loop subsystem.

covered by the leadframe and hermetically sealed with the braze. The use of a high-temperature Ag/Cu braze allows subsequent eutectic die attach and Au/Sn hermetic sealing processes. These packages have passed both the thermal shock and leakage criteria of MIL-STD-883C.

V. Leveling Loop Subsystem

The two packaged GaAs MMIC's were used as the key components to build a 1–10-GHz leveling loop subsystem. Fig. 15 shows the block diagram of the leveling loop. The external operational amplifier is used for the loop gain element in addition to the attenuator internal op-amp which controls its input match. The only off-board component used in the subsystem is a wide-band coaxial detector which can, in principle, also be surface mounted. All other components were surface mounted as shown in Fig. 16.

The use of the active splitter allowed one output port to be detected, amplified, and fed back to the attenuator, while the second port simultaneously provided the buffered leveled output. Since output port-to-port isolation is high, mismatches in the leveled output port do not influence the feedback path to the attenuator, and a stable loop results. The ultimate leveling range of the loop is set by the attenuation range of the attenuator MMIC, which depends on the highest frequency of operation desired. This range was measured to be 12 dB at 8 GHz, dropping to 9 dB at 10 GHz. Fortunately, the decreasing leveling range with frequency is not considered a disadvantage. Since most sources exhibit decreased output at higher frequencies, they require more leveling range at the lower frequencies. RF isolation from leveled output back to the source was in excess of 30 dB using the design topology presented here. Fig. 17 shows a typical response of the leveling loop in operation from 1 to 11 GHz. The source was an unleveled, swept YIG oscillator whose amplitude characteristics are

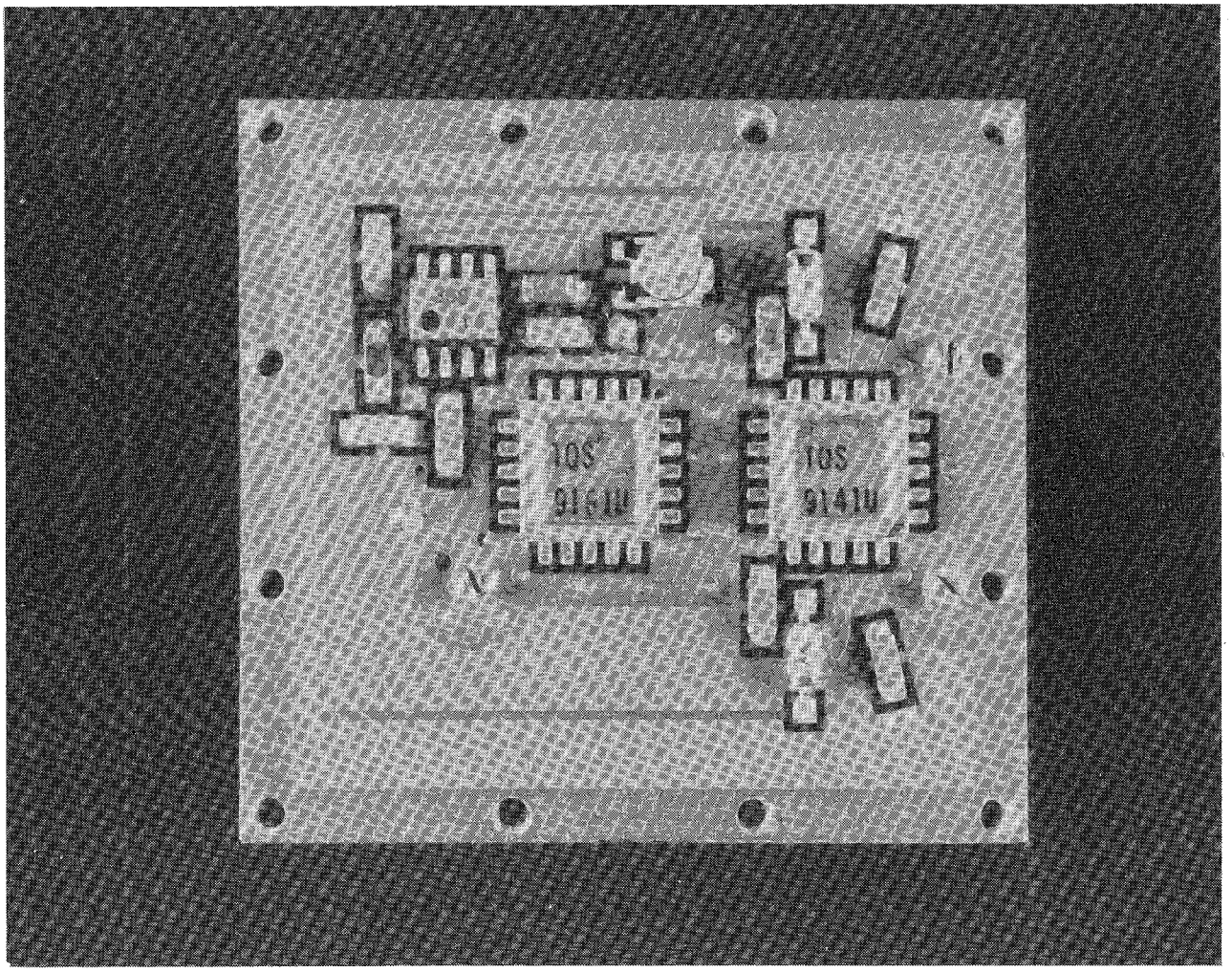


Fig. 16. Photo of the leveling loop subsystem showing the surface-mounted GaAs MMIC's.

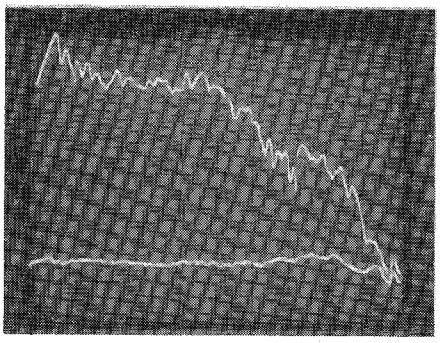


Fig. 17. Operation of the leveling loop using an unleveled swept oscillator. The input source is shown before (upper trace) and after leveling (lower trace). The vertical scale is at 2 dB/div., with 2 dBm at the center. The horizontal scale sweeps from 1 GHz to 11 GHz at 1 GHz/div.

visible in the top trace in the photo. The leveling loop utilized dominant pole compensation to set the loop bandwidth to approximately 100 kHz. This was sufficient to accommodate the relatively slowly varying power ripples in the YIG oscillator at its maximum sweep rate of 400 MHz/ms.

The packaged GaAs MMIC's were surface mounted on a 4.5-cm by 4.2-cm RT-Duroid® board, 0.079 cm (31 mils) thick, to form the leveler subsystem shown in Fig. 16. For demonstration of the leveling loop, SMA connectors provided input and output ports, with coplanar transmission lines between the MMIC's. In a typical application, these input and output connections would come from other surface-mounted components. A backside aluminum plate provides rigidity for the soft substrate, as well as thermal heat sinking for the active components.

VI. Summary

A 1–10-GHz leveling loop has been demonstrated which shows a new generation of broad-band microwave subsystem design using GaAs MMIC's. More than 30 dB of source isolation and a 9-dB leveling range at 10 GHz are attributed to the design and application of a GaAs variable attenuator and an active power splitter.

The novel attenuator circuit shown here is the first reported application of an on-chip GaAs operational amplifier in an MMIC application. This amplifier is used to internally optimize the input and output return loss as

the attenuation is varied. Packaged input and output VSWR is held to better than 1.7:1 over the entire 1–10-GHz band. Furthermore, this performance demonstrates that the addition of complex analog circuits can be used to bring increased functionality to GaAs MMIC designs.

The active splitter uses two distributed amplifiers sharing a common gate line to provide flat unity gain over the 1–10-GHz range, with reverse and port-to-port isolations exceeding 27 dB and 20 dB, respectively. Input and output VSWR's were better than 2:1, typical of the distributed amplifier topology. The active splitter concept presented here gives superior performance not found in passive splitters and couplers.

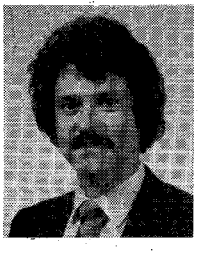
Finally, the use of surface mount packaging on soft substrates for GaAs MMIC's is projected to reduce the design and manufacturing cost of microwave systems.

ACKNOWLEDGMENT

The authors would like to acknowledge the contribution and support of P. Snow, D. Powers, T. Reeder, G. Roper, and T. Ruttan, with special thanks to E. Knapp and R. Selberg for many hours of careful measurements.

REFERENCES

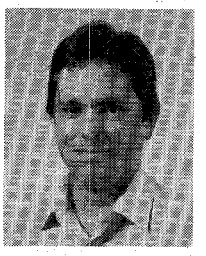
[1] A. Rode, A. McCamant, G. McCormick, and B. Vetanen, "A high-yield GaAs MSI digital IC process," in *Proc. IEEE IEDM*, 1982, pp. 162–165.
[2] *Reference Data for Radio Engineers*, 5th ed., ITT/Howard W. Sams & Co., Inc. 1968.
[3] S. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, ch. 6.
[4] L. Larson, J. Jensen, H. Levy, P. Greiling, and G. Temes, "GaAs differential amplifiers," in *Proc. 1985 IEEE GaAs IC Symp.*, pp. 19–22.
[5] J. Vorhaus, R. Pucel, and Y. Tajima, "Monolithic dual-gate GaAs FET digital phase shifter," in *Proc. 1981 IEEE GaAs IC Symp.*, paper 35.
[6] D. Pavlidis *et al.*, "A new, specifically monolithic approach to microwave power amplifiers," in *Proc. 1983 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, pp. 54–58.
[7] Y. Ayasli, L. Reynolds, R. Mozzi, and L. Hanes, "2–20 GHz GaAs traveling-wave power amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 290–295, Mar. 1984.
[8] K. Jones, G. Barta, and G. Herrick, "A 1 to 10 GHz tapered distributed amplifier in a hermetic surface mount package," in *Proc. 1985 IEEE GaAs IC Symp.*, pp. 137–140.



Gary S. Barta received the B.S. degree in physics in 1975 and the M.S.E.E. degree in 1976 from Washington State University.

In 1976, he joined the research laboratories of Tektronix, Inc., where he contributed to the design and development of high-speed silicon and GaAs charge-coupled devices and signal-processing devices. He has worked on numerous projects involving the design and development of NMOS, bipolar, and electroluminescent technologies. In 1984, he joined the Gallium Arsenide Integrated Technology research group of Tektronix, which later became TriQuint Semiconductor, Inc. His most recent responsibilities involve analog circuit and monolithic microwave IC design along with strategies for producing commercial product lines using GaAs.

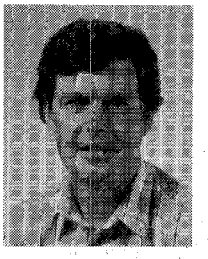
Mr. Barta is a member of Phi Beta Kappa.



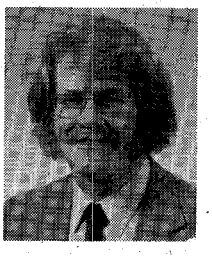
Keith E. Jones completed the B.S.E.E. at the University of Portland in 1984, and has done graduate studies in microwave engineering at the Oregon Graduate Center.

In 1974, he joined the Microwave Division of Systron-Donner, where he served as an associate engineer in the development of microwave spectrum analyzers. In 1977, he joined the Frequency Domain Instruments division of Tektronix, Inc., where he developed microwave components for spectrum analyzer front-ends. His most recent position was that of Senior Design Engineer with the Microwave Technology Organization, where he was responsible for GaAs MMIC designs. He has recently joined Cascade Microtech, Inc., as a microwave research engineer.

Mr. Jones is a member of Eta Kappa Nu.



Geoffrey C. Herrick was born in Chicago, IL, on Nov. 13, 1954. He received the B.A. degree in applied mechanics and engineering sciences from the University of California, San Diego, in 1976. He worked on the Hot Dry Rock Geothermal Program at Los Alamos Scientific Laboratories before receiving the M.S. degree in mechanical engineering from Montana State University in 1978. In his current position at Tektronix, he is responsible for the development and manufacture of GaAs MMIC packages.



Eric W. Strid (S'74–M'75) received the B.S.E.E. degree at MIT in 1974 and the M.S.E.E. degree from the University of California at Berkeley in 1975. He first worked on microwave MIC's at Farinon Transmission Systems, San Carlos, CA. In 1979, he joined the gallium arsenide research group at Tektronix, which has evolved into TriQuint Semiconductor. In 1983, he cofounded Cascade Microtech, Inc., where he is now president and CEO.

Mr. Strid has published various papers on power GaAs FET's, noise figure measurements, analog and digital GaAs IC's, and high-frequency wafer probing.